

### **REMARKS**

This responds to the Office Action mailed on February 03, 2005. Reconsideration is respectfully requested.

#### **Status of Claims**

By this amendment, claims 1, 3, 7, 10, 11, 13, 14, 17 – 21, 25 and 28 - 30 are amended, no claims are canceled, and no claims are added; as a result, claims 1 – 30 remain pending in this application.

#### **Claim Objections**

Claims 27 - 29 have been objected to for informalities. In the original application, two claim 27s were provided. Claims 27 - 29 have been amended to correct these informalities as noted by the Examiner. Claim 27 has been changed to claim 28, claim 28 has been changed to claim 29, and claim 29 has been changed to claim 30. Applicant would like to thank the Examiner for noting these informalities and giving Applicant an opportunity to correct them. The remarks below refer to the new claim numbers.

#### **Allowable Subject Matter**

Claims 3 – 7, 9, 11, 12, 14 – 17 and 21 – 30 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 3 and 7 have been rewritten in independent form including all of the limitations of the base claim 1 and are believed to be in condition for allowance. Claims 4 – 6 and 12 are believed to be in condition for allowance at least because of their dependency on now

independent claim 3. Claim 9 believed to be in condition for allowance at least because of its dependency on now independent claim 7.

Claim 11 has been rewritten in independent form including all of the limitations of the base claim 1 and intervening claim 10 and is believed to be in condition for allowance.

Claims 14 and 17 have been rewritten in independent form including all of the limitations of the base claim 13 and are believed to be in condition for allowance. Claims 15 and 16 are believed to be in condition for allowance at least because of their dependency on now independent claim 14.

Claim 21 has been rewritten in independent form including all of the limitations of the base claim 20 and is believed to be in condition for allowance. Claim 25 has been amended to be dependent on claim 21. Claims 22 – 30 are believed to be in condition for allowance at least because of their dependency on now independent claim 21.

### §102 Rejection of the Claims

Claims 1, 2, 8, 10, 13 and 18 - 20 were rejected under 35 USC § 102(b) as being anticipated by Wallace et al. (U.S. 6,137,377). Applicant's claim 1, as amended, is directed to a monolithic array amplifier and recites a plurality of amplification units arranged in a grid-like structure on a single monolithic semiconductor substrate. The monolithic array amplifier also includes a grid-bias network on the single monolithic semiconductor substrate separating the amplification units to provide DC power to the amplification units. As recited in claim 1, each amplification unit comprises bias-line bypass circuits coupling each amplification unit with the grid bias network. As recited in claim 1, the bias-line bypass circuits are arranged in a periodic structure.

Wallace, on the other hand, discloses individual semiconductor circuits that have been diced up into a large number of individual circuits and individually mounted on separate RF substrates (See Wallace's elements 410). Each module 408 is on a separate silicon ASIC. This is illustrated in FIGs 2A and 3 of Wallace which shows separate GaAs MMIC chips. Applicant's

claim 1, on the other hand, is directed to a single-monolithic substrate array amplifier.

Applicant's claim 1 recites that the plurality of amplification units are arranged on *a single monolithic substrate*. Claim 1 also recites that each of the amplification units have their own bias-line bypass circuits coupled with a common bias structure on the single substrate. This is not taught, suggested or motivated by Wallace. Wallace does not disclose any bias line bypass circuits between modules 408, nor does Wallace disclose any bias line bypass circuits between amplifiers 508 and 510. Wallace simply shows a +5v and a -5v bias line to each amplifier module 408.

Since Wallace's modules 408 are not on a single monolithic semiconductor substrate, Wallace cannot have a grid-bias network on a single monolithic semiconductor substrate separating the amplification units to provide DC power to the individual amplification units, as recited in Applicant's claim 1.

Applicant further finds no teaching, suggestion or motivation in Wallace of providing bias-line bypass circuits coupling each amplification unit with the grid bias network of the monolithic substrate. Applicant further finds no teaching, suggestion or motivation in Wallace of providing bias-line bypass circuits are arranged in a periodic structure as recited in Applicant's claim 1. An example of a periodic structure of bypass circuits 206 is illustrated in Applicant's FIG. 2. Wallace shows only providing a +5v and a -5v bias line separately to each module 108 (See Wallace FIGs. 2A and 3).

In view of the above, Applicant submits that claim 1 is not anticipated by Wallace, and that the rejection of claim 1 has been overcome. Claim 1 is believed to be in condition for allowance. Claims 13 and 20 are also believed to be allowable over Wallace for similar reasons discussed above with respect to claim 1.

Claim 2 recites that each bias-line bypass circuit is positioned along bias streets of the grid-bias network and the bias-line bypass circuits are positioned at least partially around each amplification unit within a grid unit to reduce RF current flow between an associated one of the amplification units and the grid-bias network.

Applicant finds no teaching, suggestion or motivation in Wallace of bias streets which provide bias to amplifiers on a single monolithic substrate. Wallace only discloses a +5v and a -5v bias line to the GaAs chip in FIG. 3

Applicant further finds no teaching, suggestion or motivation of bias-line bypass circuits positioned at least partially around each amplification unit within a grid unit to reduce RF current flow between an associated one of the amplification units and the grid-bias network.

In view of the above, Applicant submits that claim 2 is not anticipated by Wallace.

Applicant's claims 10, 18 and 19, for example, further distinguish over Wallace by reciting that receive and transmit antennas are part of the amplification units and that they are on the single substrate. Wallace's receive antennas 502 and 504 are clearly external to modules 408 (See Wallace FIG. 3). Furthermore, Wallace does not disclose transmit antennas associated with a module. In Wallace, signals 530 from each module 408 are provided to a combining network. In view of this, Applicant submits that claim 10, 18 and 19 are not anticipated by Wallace. Applicant's claim 19, for example, recites that the transmit antenna retransmits the signals received by the receive antenna. Applicant finds no such teachings in Wallace. In view of this, Applicant submits that claims 10, 18 and 19 are not anticipated by Wallace.

AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111

Serial Number: 10/959,794

Filing Date: October 6, 2004

Title: MOTION COMPENSATED SYNTHETIC APERTURE IMAGING SYSTEM AND METHODS FOR IMAGING

Assignee: Raytheon Company

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Dkt: PD-04W087

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the claims and the specification under 35 U.S.C. § 112, and the objection to the disclosure under 37 CFR § 1.71 with respect to the term imaging.

Conclusion

Applicants respectfully submit that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney Gregory J. Gorrie (Reg. No. 36,530) at (480) 659-3314 or Applicant's below-named representative at (520) 794-4143 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 50-0888.

Respectfully submitted,

By their Representatives,

Raytheon Company  
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Date

4.13.05

By

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 14 day of APRIL

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